FORM PTO-1083


**PATENT**
Attorney Docket No. 401251/TAKADA

In re Application of: ISHIDA et al.
Application No. 09/877,037
Filed: June 11, 2001
For: MATCHING CIRCUIT AND SEMICONDUCTOR DEVICE



**COMMISSIONER FOR PATENTS**
**Washington, D.C. 20231**

Sir:

Transmitted herewith is a response to an office action in the subject application.

☐ Applicants claim small entity status of this application under 37 CFR 1.27.

☒ Petition for Extension of Time
- ☐ Applicants petition for a one-month extension of time under 37 CFR 1.136, the fee for which is $110.00 (enclosed).
- ☒ Applicants believe that no petition for an extension of time is necessary. However, to the extent that such petition is deemed necessary, Applicants hereby petition for a sufficient extension of time to render the present submission timely. Please charge Deposit Account No. 12-1216 for the appropriate petition fee.

☒ No additional claim fee is required.

☐ Other:

The claim fee has been calculated as shown below:

| | Claims Remaining After Amendment | | Highest Number Previously Paid For | Extra Claims Present | Small Entity Rate | Small Entity Addit. Claim Fee | Other Than A Small Entity Rate | Other Than A Small Entity Addit. Claim Fee |
|---|---|---|---|---|---|---|---|---|
| Total | | Minus | | = | x 9= | $ | x 18= | $ |
| Independent | | Minus | | = | x 42= | $ | x 84= | $ |
| ☐ First Presentation of Multiple Claim | | | | | + 140= | $ | + 280= | $ |
| | | | | | Total | $ | Total | $ |

☐ Please charge my Deposit Account No. 12-1216 in the amount of $ . A duplicate copy of this sheet is attached.

☐ A check in the amount of $ is attached.

☒ The Commissioner is hereby authorized to charge any deficiencies in the following fees associated with this communication or credit any overpayment to Deposit Account No. 12-1216. A duplicate copy of this sheet is attached.
- ☒ Any filing fees under 37 CFR 1.16 for the presentation of extra claims.
- ☒ Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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Date: August 6, 2002
JAW:ves

PATENT
Attorney Docket No. 401251/TAKADA

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

ISHIDA et al.

Application No. 09/877,037 Art Unit: 2817

Filed: June 11, 2001 Examiner: W. Harris

For: MATCHING CIRCUIT AND SEMICONDUCTOR DEVICE

**PENDING CLAIMS AFTER AMENDMENTS MADE IN RESPONSE TO OFFICE ACTION DATED MAY 10, 2002**

13. A monolithic microwave integrated circuit (MMIC) comprising:

a transistor having an input terminal and an insulating film around the transistor, affecting input capacitance of the transistor, the input capacitance changing directly with thickness of the insulating film; and

a metal-insulator-metal (MIM) capacitor including two metal electrodes separated by part of the insulating film, one of the metal electrodes being connected to the input terminal of the transistor, capacitance of the MIM capacitor changing inversely with the thickness of the insulating film, whereby variations in the input capacitance of the transistor and the capacitance of the MIM capacitor due to variations in the thickness of the insulating film are compensated.

14. The MMIC according to claim 13 including a bias circuit connected in parallel with the MIM capacitor.

15. A monolithic microwave integrated circuit (MMIC) comprising:

a transistor having an output terminal and an insulating film around the transistor, affecting output capacitance of the transistor, the output capacitance changing directly with thickness of the insulating film; and

a metal-insulator-metal (MIM) capacitor including two metal electrodes separated by part of the insulating film, one of the metal electrodes being connected to the output terminal of the transistor, capacitance of the MIM capacitor changing inversely with the thickness of the insulating film, whereby variations in the output capacitance of the transistor and the capacitance of the MIM capacitor due to variations in the thickness of the insulating film are compensated.

16. The MMIC according to claim 14 including a bias circuit connected in parallel with the MIM capacitor.